

Application No. 10/016,540  
Filed: October 26, 2001  
TC Art Unit: 2182  
Confirmation No.: 7896

REMARKS

The instant Remarks are filed in response to the official action dated January 2, 2004. Reconsideration is respectfully requested.

The status of the claims is as follows:

Claims 1-14 are currently pending.

Claims 1-14 stand rejected.

The Examiner has rejected claims 1-6 and 8-14 under 35 U.S.C. 102(e) as being anticipated by Ducaroir et al. (USP 6,167,077). Specifically, the official action indicates, in relevant part, that the Ducaroir reference teaches a method of transmitting parallel data to a destination over a plurality of serial data lines including the steps of transmitting a clock signal to the destination over a clock line in parallel with the plurality of serial data lines, the clock signal having at least one data bit of each parallel data word encoded thereon, and aligning regenerated parallel data words using the respective data bits encoded on the clock signal. The Applicants respectfully submit, however, that Ducaroir et al. do not describe the limitations of each and every element or step of base claims 1 and 8, and therefore the Ducaroir reference does not anticipate claims 1 and 8 and the claims dependent therefrom.

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For example, Ducaroir et al. neither teach nor suggest a method of transmitting parallel data that includes transmitting a clock signal to a destination over a clock line in parallel with a plurality of serial data lines, in which the clock signal has at least one data bit of each parallel data word encoded thereon, and subsequently aligning regenerated parallel data words using the respective data bits encoded on the clock signal, as recited in base claims 1 and 8. The notion of encoding alignment information for parallel data on a clock that is transmitted to a destination over a high speed serial line in parallel with serial data representative of the parallel data is described throughout the instant application, e.g., see page 3, line 28, to page 4, line 2; page 4, line 27, to page 5, line 4; and, page 5, lines 27-30, of the application.

Like the instant application, the Ducaroir reference relates to the transmission of parallel data to a destination using multiple high speed serial lines. The Applicants respectfully submit, however, that Ducaroir et al. employ a technique for aligning the parallel data recovered at the destination that is significantly different from the technique disclosed in the instant application and recited in base claims 1 and 8. The Ducaroir reference actually describes two alignment techniques,

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both of which use what Ducaroir calls a "training pattern". Specifically, in a first alignment technique, the training pattern is transmitted to the destination over the multiple serial lines as a plurality of data sets. Next, data skew is measured across, between, or among the data sets, and a "preskew" pattern is determined which when integrated into the training pattern results in the training pattern being received properly when retransmitted. The preskew pattern is then fed back to the transmitter and integrated into all subsequent data sets before transmission (see column 6, lines 32-42, of Ducaroir et al.).

A second alignment technique described by Ducaroir et al. uses the above-mentioned training pattern in conjunction with alignment buffers in data and clock recovery units at the destination. Specifically, the data and clock recovery units are directed to align the training pattern, and all subsequent data sets, in the alignment buffers for correct reception of the data bits. This second alignment technique has the advantage of not requiring a feedback channel for the preskew pattern (see column 6, lines 60-67, of Ducaroir et al.).

Although the official action purportedly indicates that the Ducaroir reference describes a clock, e.g., the clock 120A, which might have at least one data bit of each parallel data word

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encoded thereon (see column 4, lines 19-40, and Fig. 1, of Ducaroir et al.), the Applicants respectfully submit that not only does the clock 120A have no bits of the parallel data encoded thereon, but the clock 120A is not used to align the data. Instead, Ducaroir et al. describe using the clock 120A to deserialize the serialized data (see column 4, lines 35-37, of Ducaroir et al.).

In fact, the Ducaroir reference teaches away from encoding alignment information for parallel data on a clock transmitted to a destination over one of a plurality of high speed serial lines, as disclosed in the instant application. For example, as mentioned above, the alignment technique employed by Ducaroir et al. includes employing a training pattern to generate a preskew pattern, which is subsequently fed back to the transmitter. Significantly, the bits of the preskew pattern are not integrated into a clock (such as the clock 120A), but are instead integrated into all subsequent data sets before transmission (see column 6, lines 32-42, of Ducaroir et al.). This is essentially opposite to the alignment technique that is disclosed and claimed in the instant application, which describes the drawbacks of integrating alignment information into the data to be transmitted, e.g., it may result in wider data words requiring higher transmission rates

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to achieve a desired level of performance (see page 3, lines 6-11, of the application). The method and system of transmitting parallel data recited in base claims 1 and 8 avoids this drawback by encoding alignment information not within the data, but rather on a clock transmitted with the data over respective high speed serial lines (see page 3, line 28, to page 4, line 2, of the application).

Because the Ducaroir reference does not describe encoding at least one data bit of each parallel data word on a clock signal, and aligning regenerated parallel data words using the respective data bits encoded on the clock signal, as recited in base claims 1 and 8, the Ducaroir reference does not anticipate claims 1 and 8 and the claims dependent therefrom. Accordingly, the Applicants respectfully submit that the rejections of claims 1-6 and 8-14 under 35 U.S.C. 102 are unwarranted and should be withdrawn.

The Examiner has rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Ducaroir et al. in view of Lecourtier et al. (USP 6,560,275). The Applicants respectfully assert, however, that the Lecourtier reference does not cure the above-described deficiencies of the Ducaroir reference, and therefore the suggested combination of the Ducaroir and Lecourtier references does not render dependent claim 7 obvious.

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For example, the Lecourtier reference does not describe encoding a data bit of respective parallel data words on a clock signal, and aligning the parallel data words using the data bits encoded on the clock signal, as recited in base claims 1 and 8. In fact, the Lecourtier reference is similar to the Ducaroir reference in that it describes achieving digital synchronization of frames through a digital alignment of recognition patterns, i.e., "start bits", contained in the starts-of-frame provided according to the SDH data transport protocol (see column 4, lines 28-32, of Lecourtier et al.). Such alignment techniques that employ "preskew patterns" or "recognition patterns", as described in the Ducaroir and Lecourtier references, are not suggestive of the technique in which alignment information is encoded onto a clock, as recited in base claims 1 and 8.

Because the disclosure of the Lecourtier reference does not cure the deficiencies of the Ducaroir reference, the suggested combination of the Ducaroir and Lecourtier references does not render dependent claim 7 obvious. Accordingly, the rejection of claim 7 under 35 U.S.C. 103 is unwarranted and should be withdrawn.

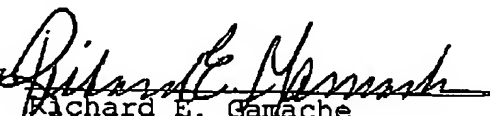
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In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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